International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622
International Conference On Emerging Trends in Mechanical and Electrical Engineering (ICETMEE-13th-14th March 2014)

RESEARCH ARTICLE OPEN ACCESS

CMOS Domino Logic Circuit for High Speed Performance

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Abstract
In this paper a high speed and low power domino logic circuit is proposed by using voltage divider current mirror technique. To avoid charge leakage and charge sharing problems, domino logic design is used in the circuit due to their advantages such as high speed and less noise immunity. Using this voltage divider current mirror circuit, contention current and power dissipation in the circuit is reduced without affecting the noise immunity of the circuit. With the scaling in technology, performance of digital logic is degrades due to increase in sub-threshold current. This proposed circuit provides very small speed-power product as compared to previously designed domino logic circuits. Simulations are carried out in cadence 90nm technology with supply voltage of 1 volt for the case of OR gate.
Keywords: *evaluation phase, pre-charge phase,dynamic node, robustness*

I. Introduction

Domino logic circuits with wide fan-in are widely used in digital circuit designs due to their high speed and less number of transistors. Footless domino gate is most popular due to their less transistors count and better performance in comparison with static CMOS [1][2][3]. Footless domino gates are very simple to be realized in case of wide fan-in. Wide fan-in footless domino logic are often implemented in data-path in microprocessors, digital signal processing and digital memories. There are different sources in digital circuits. Most common noise sources are crosstalk, variation in supply voltage, charge leakage and charge redistribution [4]. The most effective way to reduce power dissipation is to reduce supply voltage. However on reducing supply voltage, threshold voltage is also reduced, which leads to increase in sub-threshold current exponentially [5].

The dynamic node of domino gate is affected by noise during evaluation phase. Dynamic node of domino gate can still discharge through Pull Down Network due to phenomena of charge leakage, charge redistribution and charge sharing [6]. Due to leakage current and noise in pull down network dynamic node of domino logic is discharged in evaluation phase. To hold the state of dynamic node during evaluation phase, keeper circuit is used at dynamic node. Generally a

PMOS transistor is used in feedback as keeper circuit [7][8]. PMOS keeper prevents the charge stored at dynamic node during evaluation phase, when the inputs of pull down network are zeros.
However, if the intensity of sub-threshold current is high keeper may not be able to maintain charge at the dynamic node. Keeper circuit provides contention current and thus degrades the performance of circuit. Due to generation of contention current short-circuit power is dissipated in the keeper circuit [9].

Keeper circuitry should be designed such that it will provide high performance, minimum contention current, less power consumption, less area and robustness. The basic dynamic domino gate is shown in fig1. When clk is low, M_p is turned ON, dynamic node charges to V_{dd} and circuit is in pre-charge state. Because M_n is turned OFF, there does not exist any path to ground. When clk is high, transistor During evaluation phase, there are two conditions for the output voltage. If inputs IN1 and IN2 are equal to one, the dynamic node value is equal to zero and output of the circuit will be equal to one. When both input values are equal to zero, dynamic node voltage should be maintained at high value and output of the circuit should be zero. In this proposed scheme of domino logic, voltage divider current mirror circuit is used to

improve power-delay product and noise immunity.

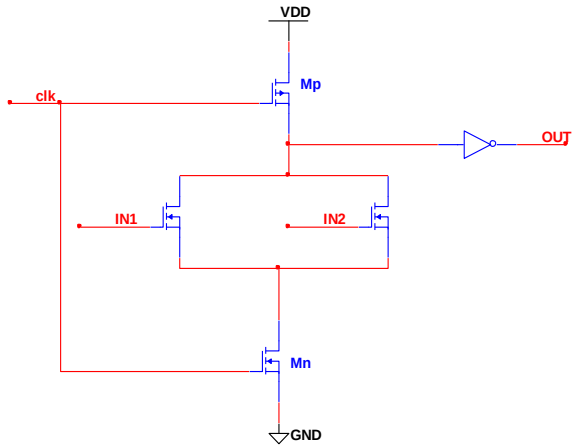

Fig.1 Domino logic circuit without keeper

This paper is organized as follows. Section [II] describes the problem statement related to leakage current and noise. Section [III] represents previous work done related to dynamic logic. Section [IV] presents proposed domino logic circuit scheme and simulation results. Conclusion is presented in section [VI].

II. Problem Statement

Major problem arises in domino logic circuit during evaluation phase, when both the inputs of pull down network are zeros. During this period, charge leakage phenomenon takes place in the circuit and sub-threshold leakage current becomes very dominant in the pull down network. Band-to-band tunneling current flows in pull down network, when gate to source voltage of pull down network is less than that of threshold voltage [9].

To reduce leakage current in pull down network, either threshold voltage of NMOS of PDN should be increased or size of NMOS pull down network should be increased [9]. However during evaluation phase on increasing threshold voltage, discharging current in pull down network is reduced.
Fig.2 shows that When clock is low, PMOS will turn ON, and dynamic node will be charge up to V_{dd} and circuit is in pre-charge phase. When clock is high, PMOS will turn OFF, and there exists two conditions of output depending on the inputs (1) if inputs are high, charge stored at dynamic node will be discharge through ground. (2) if inputs are low, charge stored at dynamic node must be maintained at the node. Because of charge redistribution problem, NMOS pull down network leaks the charge stored at dynamic node. By using PMOS keeper transistor at dynamic node, the contention current problem also reduces. However, due to presence of noise signal at the gate of pull down network, if PDN is activated during evaluation period, it will wrongly discharge the dynamic node [10].

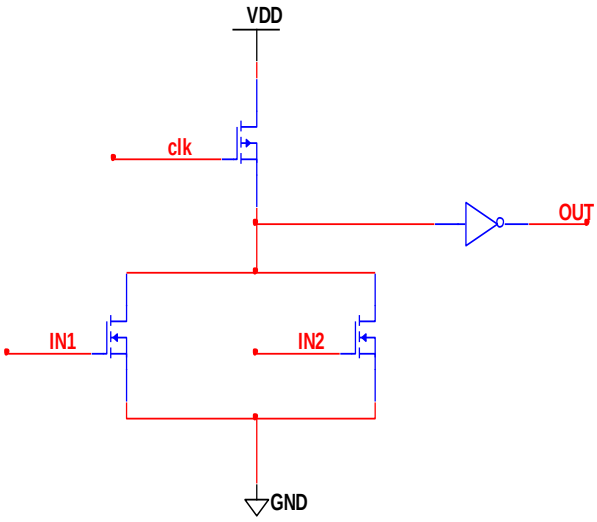

Fig.2 Basic domino logic circuit

III. Previous Background Work

Noise impulses at the input of NMOS pull down network increases the gate to source voltage. So that sub-threshold current increases the charging of dynamic node [11]. Due to this process gate-to-source voltage of the active NMOS decreases and the sub-threshold leakage current is exponentially reduced. Keeper circuit is used in domino logic to eliminate sub-threshold leakage current at dynamic node. When pull down network is turned OFF, keeper circuit prevents the charge stored at dynamic node in evaluation phase.Three conventional designs of domino logic circuits includes Footless domino logic circuit, footer domino logic circuit, and high speed domino logic circuit. Domino logic scheme is basically proposed for high speed, less area, and low power application. However, dynamic node of domino gate is susceptible to noise source, which causes serious design challenges. To prevent charge stored at dynamic nod, keeper circuit is used. On increasing size of PMOS keeper robustness of the circuit increases at the cost of power dissipation and delay [12].

Footless domino logic and footer domino logic are shown in the Fig.3 and Fig.4 respectively. Footless domino logic is very simple in design and easy to use. Footer domino logic becomes more noise immune than footless domino logic, due to footer transistor added at the bottom of evaluation network [13][14]. However speed of footless domino logic is more than that of footer domino logic. There is a finite

resistance presents in footer transistor, due to which performance of domino logic circuit degrades in evaluation phase.

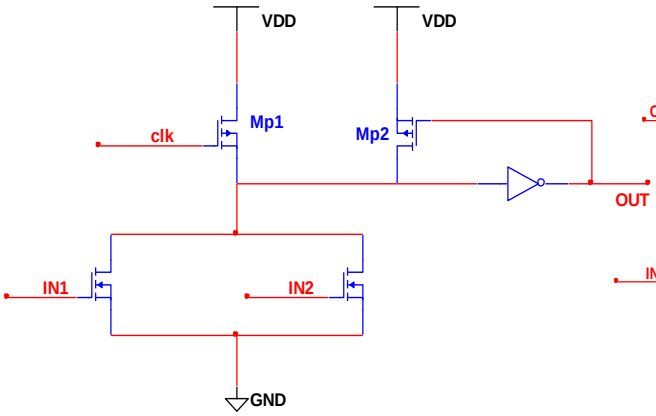

Fig.3 Footless domino logic

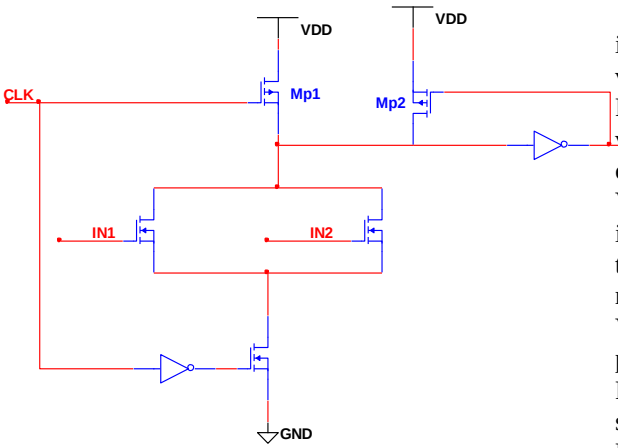

Fig.4 Footer domino logic

Fig.5 shows high speed domino logic circuit. High speed domino logic is more leakage tolerant than footless and footer domino logic circuits. At the beginning of evaluation phase PMOS transistor Mp3 is and therefore keeper transistor Mp2 is off. After a delay equal to delay of inverters, when clk becomes high, if the output node is high Mn1 remains off and keeper transistor Mp2 also remains off. However, if output is low after a delay equal to delay of inverters in evaluation phase, dynamic node is connected to output node via inverter [15]. This causes keeper PMOS Mp2 to keep dynamic node connected to $v_{dd.}$

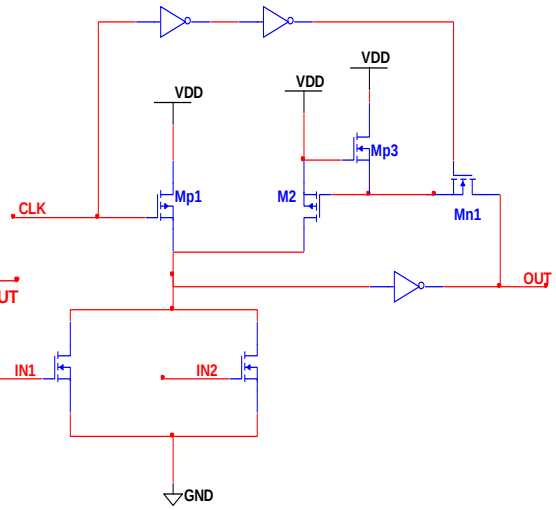

Fig.5 High speed domino logic circuit

IV. Proposed Domino Logic Circuit

The proposed domino logic scheme is shown in Fig.6 In this circuit in place of footer transistor voltage divider based current mirror circuits are used. Principle of current mirror is s that, if gate to source voltage of two identical transistors are equal, then the current flown through their drains should be equal. Voltage divider current mirror circuit provides insensitivity for supply voltage variations and temperature variations. Voltage divider based current mirror used for small current biasing applications. Voltage divider current mirror circuit consumes low power as compared to other current mirror circuits [16]. Purpose of current mirror circuits that, if any noise signal occurs at M1 it will be leak to ground via M4 and M5. Due to both current mirror circuits gate to source voltage of NMOS pull down network decreases rapidly. Transistors M1 and M3also provide stacking effect. Due to stacking effect gate to source voltage of NMOS pull down network is reduce [18]. Purpose of transistor Mp1 is to provide strong v_{dd} to the lower PMOS because PMOS transistor is used to provide strong one to the logic circuits.

The presence of voltage divider current mirror in the proposed circuit causes increase in delay. To overcome this problem size(W/L ratio) of PDN should be increased. Because of stacking effect circuit dissipates power and becomes less noise robust [18]. In this proposed circuit there will be voltage drop in evaluation phase due to stacked transistors M2 and M4. Due to negative V_{gs}, there will be exponential reduction in subthreshold current in the circuit, because sub-threshold current has exponentialmrelation with gate to source voltage.In order to improve power-delay

product more and more, size of PMOS transistor of inverter at output node should be four times that of NMOS transistor. Circuit is simulated with clock frequncy of 2nhtz and supply voltage of 1volt. Simulation results showes that on reducing supply voltage power of the circuit reduces but delay of the circuit increases.On increasing size of NMOS pull-down network , delay is reduces but speed-power product gradually increases. Mp2 is used to provide strong VDD to the circuit, because PMOS transistor is used to provide strong one to the circuit.

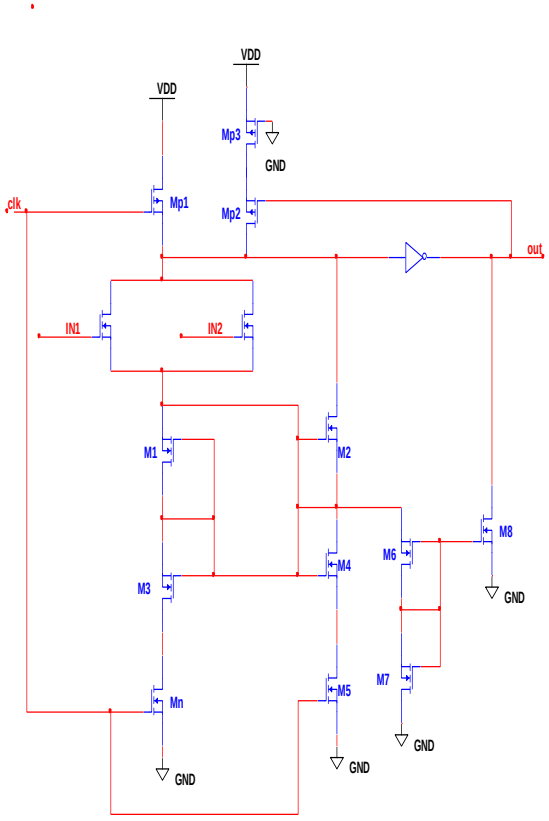

Fig.6 Proposed Domino Logic Circuit

V. Simulation Results

Fig.8 show that power-delay of proposed circuit product reduces with the increase in size of pull down network. On increasing the size of pull down network delay of the circuit is reduces. When width of PDN is 400nm, power-delay product becomes lowest in the circuit. Fig.8 shows variation in power-delay product with size of transistor M8 and pull down network for the supply voltage of 1volt. It can be concluded that when size of M8 and size of PDN is 400nm circuit gives best value of power-delay product. This proposed circuit gives lowest power-delay product for supply voltage of 1volt. Fig.9 and Fig.10 shows variation in power-delay product with size of transistor M8 and pull down network for the supply voltage of 0.9volt and 0.8 volt respectively. It can be concluded that when size of M8 and size of PDN is 400nm circuit gives best value of power-delay product. For supply voltage of 0.9 volt, power-delay product is degrades. This proposed can be scaled down for the supply voltage of 0.7 volts, but on reducing supply voltage, power and delay of the circuit is degraded because leakage current comes under effect. Delay in the circuit increases very rapidly. Delay of the circuit is increases by using current mirror, to avoid this, transistor M8 is used. On increasing the size of transistor M8, delay of the circuit is reduced to a very low value. From the table it is concluded that power-delay product of proposed circuit is very less as compared to footless domino logic, footer domino logic and high speed domino logic circuits.

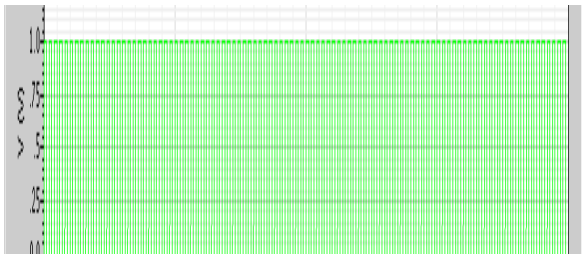

Fig.6(a) clk input

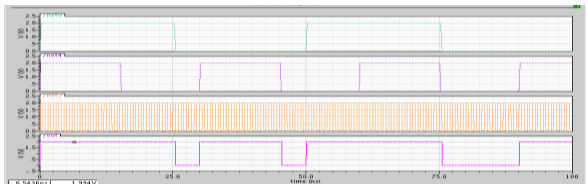

Fig.7(b) basic domino logic circuit

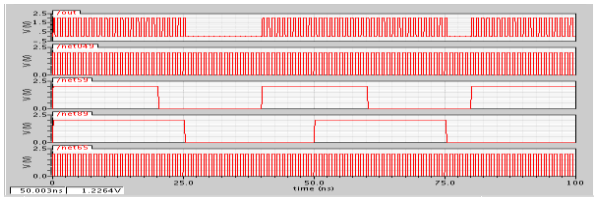

Fig.7(c) Footless domino logic circuit

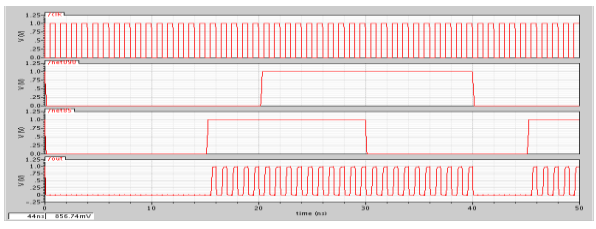

Fig.7(d) Footer domino logic circuit

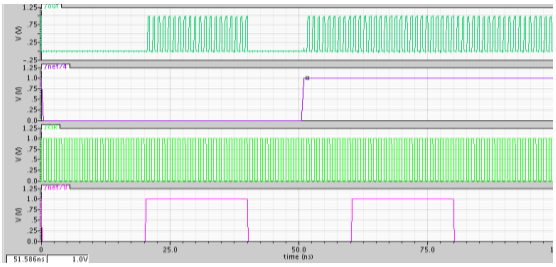

Fig.7(e) Proposed Domino Logic Circuit

Table I. Power, delay and power-delay product of different domino style circuits

	Basic domino logic	Footless domino logic	Footer domino logic	High speed domino logic	Proposed domino logic
Supply voltage	1v	1v	1v	1v	1v
power	1.33E-5	7.84E-5	5.8E-6	3.67E-4	1.24E-6
delay	3.38E-10	1.55E-10	1.03E-10	7.38E-11	2.10E-13
PDP	4.5E-15	1.21E-15	5.97E-16	6.38E-1	2.6E-19

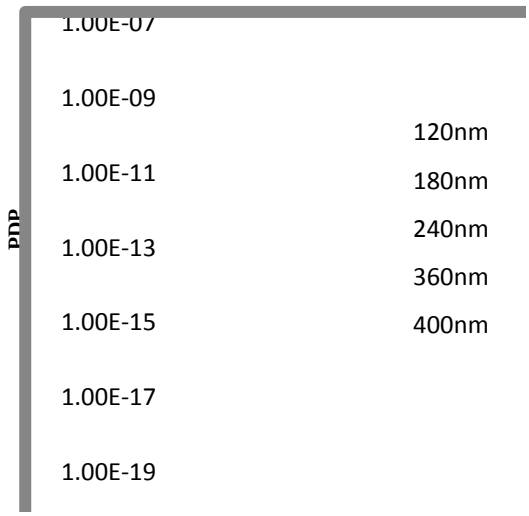

Fig.8 Variation in power-delay product with the size of pull down
network for 1volt.

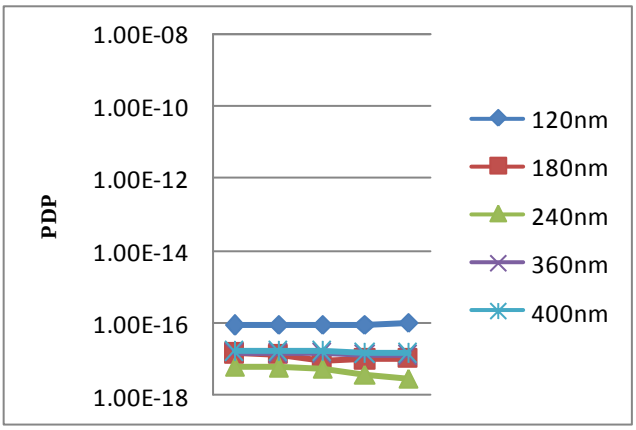

Fig.9 Variation in power-delay product with the size of pull down
network for 0.9 volt.

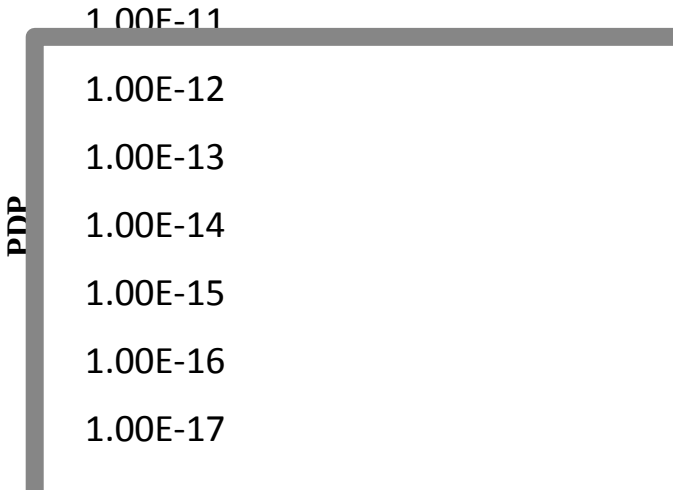

Fig.10 Variation in power-delay product with the size of pull down
network for 0.8 volt.

VI. Conclusion

In this paper a new approach for reduction in speed- power product is demonstrated. The percentage reduction in delay can be increased by either increasing threshold voltage of the inverter place at output or by reducing threshold voltage of NMOS transistors of pull down network. Another version of this proposed circuit can be implemented with the NMOS of pull down network connected in series. The proposed scheme improves both noise margin and speed at the cost of adding only two current mirrors in stack. The proposed circuit is simulated on cadence 90nm technology. Proposed circuit when compared to previous domino logic scheme, shows reduction in speed-power product, as well as improved noise immunity. The proposed

scheme is used in recent embedded processors where low power and high speed is required.

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